REMARKS

Applicant has amended claims 2 and 9 to overcome the claim objection made by the examiner. In addition, for claims 1-2, 9 and 11-21, Applicant has amended the status identifiers of these claims as suggested by the examiner.

PRIOR ART REJECTIONS

In response to the rejection of claims 1-2, 4-5, 7, and 9-21 under 35 USC 103 as being unpatentable over U.S. Patent 5,587,962 to Hashimoto et al. ("Hashimoto") in view of U.S. Patent 5,973,664 to Badger ("Badger") further in view of U.S. Patent 6,904,473 to Bloxham et al. ("Bloxham"), Applicants respectfully traverse the rejection because the combination of prior art does not disclose or suggest each claim element of the claims and therefore a prima facie case of obviousness has not been established and the rejection should be withdrawn.

Claim 1

Claim 1 has several claim elements that are not disclosed or suggested by the combination of the prior art.

"Operating the Driving Circuit" Claim Element

Claim 1 recites "operating the driving circuit in an address sequence mode wherein the address sequencer generates addresses for the video data in the memory by combining line pointers that are read out by a line counter from a block of line pointers in address table register means with the output of a pixel counter using an adder, and in a table update mode wherein a block of line pointers from the full table of line pointers that is stored in said memory is downloaded into said address table register means" which is not disclosed or suggested by the combination of Hashimoto, Badger and Bloxham for the reasons below.

Hashimoto discloses a driving circuit that has a memory circuit 14 that can operate in a random access mode and a serial mode. *See Hashimoto at col. 4, lines 8-17.* In Hashimoto, the entire table used by the driving circuit is stored in the memory (see pg. 2, lines 23-30 of the present application that describes this aspect of Hashimoto) so that Hashimoto does not perform the claimed table update mode. Thus, Hashimoto clearly does not disclose or suggest the

claimed driving circuit that operates in both an address sequence mode and also in a table update mode. Thus, Hashimoto does not disclose or suggest this claim element.

Badger discloses values being combined with an adder are not line pointers and pixel counters, as recited by claim 1. In Badger element 806, Mem_pointer is incremented by a pixel size amount, Screen_pointer is incremented by an X_increment amount, and X_counter is decreased by 1 (See Berger Col. 8 lines 34-39). In Berger element 810, Screen_Pointer is incremented by Y_Increment, and a value equal to X_Increment times Logical_Width is subtracted from Screen_Pointer. Finally in 810, Y_counter is decreased by 1 (See Berger Col. 8 lines 40-60). None of these recitations in Badger element 806 or 810, or anywhere in Badger, discloses the recitation of claim 1 above. Thus, Badger also does not disclose or suggest the claimed driving circuit that operates in both an address sequence mode and also in a table update mode.

Bloxham discloses reading data stored consecutively into a memory. Thus, Bloxham also does not disclose or suggest the claimed driving circuit that operates in both an address sequence mode and also in a table update mode.

Thus, the combination of Hashimoto, Badger and Bloxham do not disclose or suggest this claim element and the obviousness rejection should be withdrawn for at least this reason.

Table Update Mode Claim Element

Claim 1 also recites "wherein operating the driving circuit in the table update mode includes: setting a base address of the block of line pointers to zero; reading a line pointer that corresponds to the base address of zero from the memory into the address table register means; and successively increasing the base address by one and reading the corresponding line pointer from the memory into the address table register means until the last line pointer of the block of line pointers is downloaded into the address table register means" which is not disclosed or suggested by the combination of Hashimoto, Badger and Bloxham for the reasons below.

Hashimoto discloses a driving circuit that has a memory circuit 14 that can operate in a random access mode and a serial mode. *See Hashimoto at col. 4, lines 8-17.* In Hashimoto, the entire table used by the driving circuit is stored in the memory (see pg. 2, lines 23-30 of the present application that describes this aspect of Hashimoto) so that Hashimoto does not perform

the claimed table update mode. Thus, Hashimoto clearly does not disclose or suggest the particular processes for table update as recited in claim 1. Thus, Hashimoto does not disclose or suggest this claim element.

Badger discloses values being combined with an adder are not line pointers and pixel counters, as recited by claim 1. In Badger element 806, Mem_pointer is incremented by a pixel size amount, Screen_pointer is incremented by an X_increment amount, and X_counter is decreased by 1 (See Berger Col. 8 lines 34-39). In Berger element 810, Screen_Pointer is incremented by Y_Increment, and a value equal to X_Increment times Logical_Width is subtracted from Screen_Pointer. Finally in 810, Y_counter is decreased by 1 (See Berger Col. 8 lines 40-60). None of these recitations in Badger element 806 or 810, or anywhere in Badger, discloses the recitation of claim 1 above. Thus, Badger also does not disclose or suggest the claimed table update mode processes.

Bloxham discloses reading data stored consecutively into a memory. Thus, Bloxham also does not disclose or suggest the claimed table update mode processes.

Summary

Thus, the combination of Hashimoto, Badger and Bloxham do not disclose or suggest these claim elements and the obviousness rejection should be withdrawn for at least this reason.

Claims 11, 14, 16 and 19

These claims depend from claim 1 and these claims are not obvious over the combination of prior art cited by the examiner for at least the same reasons as claim 1 above.

Claim 2

Claim 2 has several claim elements that are not disclosed or suggested by the combination of the prior art.

Means for Successively Updating the Table Claim Element

Claim 2 recites "means for successively updating the address table register means with subsequent blocks of line pointers from the full table of line pointers that is contained in the memory, wherein the means for successively updating the address table register means with the subsequent blocks of line pointers is configured to set a base address of a block of line pointers

to zero, to read a line pointer that corresponds to the base address of zero from the memory into the address table register means, to successively increase the base address by one and to read the corresponding line pointer from the memory into the address table register means until the last line pointer of the block of line pointers is downloaded into the address table register means" which is not disclosed or suggested by the combination of Hashimoto, Badger and Bloxham for the reasons below.

Hashimoto discloses a driving circuit that has a memory circuit 14 that can operate in a random access mode and a serial mode. *See Hashimoto at col. 4, lines 8-17.* In Hashimoto, the entire table used by the driving circuit is stored in the memory (see pg. 2, lines 23-30 of the present application that describes this aspect of Hashimoto) so that Hashimoto does not perform the claimed table update mode. Thus, Hashimoto clearly does not disclose or suggest the particular processes for table update as recited in claim 2. Thus, Hashimoto does not disclose or suggest this claim element.

Badger discloses values being combined with an adder are not line pointers and pixel counters, as recited by claim 1. In Badger element 806, Mem_pointer is incremented by a pixel size amount, Screen_pointer is incremented by an X_increment amount, and X_counter is decreased by 1 (See Berger Col. 8 lines 34-39). In Berger element 810, Screen_Pointer is incremented by Y_Increment, and a value equal to X_Increment times Logical_Width is subtracted from Screen_Pointer. Finally in 810, Y_counter is decreased by 1 (See Berger Col. 8 lines 40-60). None of these recitations in Badger element 806 or 810, or anywhere in Badger, discloses the recitation of claim 2 above. Thus, Badger also does not disclose or suggest the claimed table update mode processes.

Bloxham discloses reading data stored consecutively into a memory. Thus, Bloxham also does not disclose or suggest the claimed table update mode processes.

Switching Means Claim Element

Claim 2 also recites "switching means, by which memory addresses for video data are generated in an address sequence mode in the address sequencer, and in a table update mode the address table register is updated with a next block of line pointers from the full table of line

pointers that is contained in the memory" which is not disclosed or suggested by the combination of Hashimoto, Badger and Bloxham for the reasons below.

Hashimoto discloses a driving circuit that has a memory circuit 14 that can operate in a random access mode and a serial mode. *See Hashimoto at col. 4, lines 8-17.* In Hashimoto, the entire table used by the driving circuit is stored in the memory (see pg. 2, lines 23-30 of the present application that describes this aspect of Hashimoto) so that Hashimoto does not perform the claimed table update mode. Thus, Hashimoto clearly does not disclose or suggest the claimed switching means that operates in both an address sequence mode and also in a table update mode. Thus, Hashimoto does not disclose or suggest this claim element.

Badger discloses values being combined with an adder are not line pointers and pixel counters, as recited by claim 2. In Badger element 806, Mem_pointer is incremented by a pixel size amount, Screen_pointer is incremented by an X_increment amount, and X_counter is decreased by 1 (See Berger Col. 8 lines 34-39). In Berger element 810, Screen_Pointer is incremented by Y_Increment, and a value equal to X_Increment times Logical_Width is subtracted from Screen_Pointer. Finally in 810, Y_counter is decreased by 1 (See Berger Col. 8 lines 40-60). None of these recitations in Badger element 806 or 810, or anywhere in Badger, discloses the recitation of claim 1 above. Thus, Badger also does not disclose or suggest the claimed switching means that operates in both an address sequence mode and also in a table update mode.

Bloxham discloses reading data stored consecutively into a memory. Thus, Bloxham also does not disclose or suggest the claimed switching means that operate in both an address sequence mode and also in a table update mode.

Thus, the combination of Hashimoto, Badger and Bloxham do not disclose or suggest this claim element and the obviousness rejection should be withdrawn for at least this reason.

Summary

Thus, the combination of Hashimoto, Badger and Bloxham do not disclose or suggest these claim elements and the obviousness rejection should be withdrawn for at least this reason.

Claims 4-5, 7, 10, 12, 15, 18 and 21

These claims depend from claim 2 and these claims are not obvious over the combination of prior art cited by the examiner for at least the same reasons as claim 2 above.

Claim 9

Claim 9 recites "means for successively updating the address table register means with subsequent blocks of line pointers from the full table of line pointers that is contained in the memory, ~~,~~ wherein the means for successively updating the address table register means with the subsequent blocks of line pointers is configured to set a base address of a block of line pointers to zero, to read a line pointer that corresponds to the base address of zero from the memory into the address table register means, to successively increase the base address by one and to read the corresponding line pointer from the memory into the address table register means until the last line pointer of the block of line pointers is downloaded into the address table register means" which is not disclosed or suggested by the combination of Hashimoto, Badger and Bloxham for the reasons below.

Hashimoto discloses a driving circuit that has a memory circuit 14 that can operate in a random access mode and a serial mode. *See Hashimoto at col. 4, lines 8-17.* In Hashimoto, the entire table used by the driving circuit is stored in the memory (see pg. 2, lines 23-30 of the present application that describes this aspect of Hashimoto) so that Hashimoto does not perform the claimed table update mode. Thus, Hashimoto clearly does not disclose or suggest the particular processes for table update as recited in claim 9. Thus, Hashimoto does not disclose or suggest this claim element.

Badger discloses values being combined with an adder are not line pointers and pixel counters, as recited by claim 9. In Badger element 806, Mem_pointer is incremented by a pixel size amount, Screen_pointer is incremented by an X_increment amount, and X_counter is decreased by 1 (See Berger Col. 8 lines 34-39). In Berger element 810, Screen_Pointer is incremented by Y_Increment, and a value equal to X_Increment times Logical_Width is subtracted from Screen_Pointer. Finally in 810, Y_counter is decreased by 1 (See Berger Col. 8 lines 40-60). None of these recitations in Badger element 806 or 810, or anywhere in Badger, discloses the recitation of claim 1 above. Thus, Badger also does not disclose or suggest the claimed table update mode processes.

Bloxham discloses reading data stored consecutively into a memory. Thus, Bloxham also does not disclose or suggest the claimed table update mode processes.

Thus, the combination of Hashimoto, Badger and Bloxham do not disclose or suggest these claim elements and the obviousness rejection should be withdrawn for at least this reason.

Claims 13, 17, 20

These claims depend from claim 9 and these claims are not obvious over the combination of prior art cited by the examiner for at least the same reasons as claim 9 above.

CONCLUSION

In view of the above, it is respectfully submitted that claims 1-2, 4-5, 7, and 9-21 as amended are allowable over the cited art and are now in condition for formal allowance, and early and favorable action to that end is respectfully requested.

The Examiner is encouraged to call Applicants' attorney at the number below if doing so will in any way advance prosecution of this application.

The Commissioner is hereby authorized to charge any fees which may be required, or credit in the overpayment, to Deposit Account No. **07-1896** referencing Attorney Docket No. **348162-982280**.

Respectfully submitted,
DLA PIPER LLP (US)

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